IN THE SPECIFICATION

Page 8, replace the heading "DISCLOSURE OF THE INVENTION" with --SUMMARY OF THE INVENTION--

Page 8, replace the paragraph appearing in lines 9-18 with the following paragraphs:

An array speaker system ~~of this invention is constituted in such a way that~~ has a plurality of speaker units arranged in an array. The speaker units are supplied with signals having prescribed time differences ~~are supplied with respect to a plurality of speaker units arranged in an array, thus controlling~~ or delay times to control the directivities of audio signal beams emitted from the speaker units. This array speaker system ~~is constituted by a delay control circuit (i.e., an audio signal beam control circuit) comprising~~ includes a delay memory having a plurality of delay taps for delaying ~~an~~ input ~~signal (i.e., an~~ audio signals[[)]] in units of sampling ~~frequency~~ periods and an interpolation processing means for outputting delay-imparted signals based on the input signals ~~executing interpolation processing on delay signals, which are extracted~~ from the delay taps of the delay memory. The array speaker system further includes means for supplying the delay-imparted signals to the speaker units, and control means for calculating the delay time supplied to the signal output ~~based on delay times calculated by a control means (i.e., a microcomputer), wherein the output of the interpolation processing means is supplied~~ to each of the speaker units.

The interpolation processing means includes at least two multipliers for multiplying outputs of at least two of the delay taps from the delay memory by coefficients supplied from the control means and an adder for adding outputs of the at least two multipliers with respect to each speaker unit.

The control means divides the calculated delay time by the sampling period, and selects at least two delay taps from the delay memory on the basis of a position corresponding to a division result so that the outputs thereof are supplied to the at least two multipliers, to set the coefficients for performing linear interpolation or Lagrange's interpolation based on the division result with respect to the multipliers.

In one embodiment, the interpolation processing means includes two multipliers for multiplying outputs of the selected two delay taps from the delay memory, and the control means selects the two taps in the delay memory on the basis of a position corresponding to a division result so that the outputs thereof are supplied to the two multipliers, to set the

coefficients for performing linear interpolation based on the division result with respect to the multipliers.

In another embodiment, the interpolation processing means includes at least three multipliers for multiplying outputs of the at least three delay taps selected from the delay memory, and the control means selects the at least three taps from the delay memory on the basis of a position corresponding to a division result so that the outputs thereof are supplied to the at least three multipliers, to set the coefficients for performing Lagrange's interpolation of two or more orders based on the division result with respect to the at least three multipliers.